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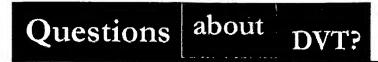
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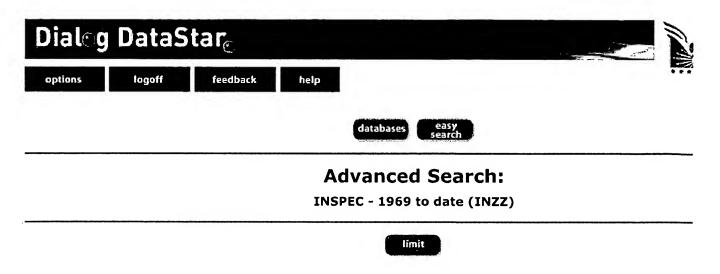
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Transactions...Dynamics of Bistable Flip-Flops", 6th Int. Symp...Davies,

...Synchronizers Operating in Metastable Region", IEEE



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CE Cummings, P Alfke - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com

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SAME 2004

S Bernardi, S Lebailly, T Instruments, B Blanc, G ... - signal - same-conference.org ... top-level is valid for **simulation** and verification ... reduction of compilation and **synthesis** time • Better ... or hold time; thus, causing a **metastable** condition and ... <u>View as HTML - Web Search - same-conference.com</u>

Using hierarchical clock tree synthesis to generate balanced clock trees

P Ragon, A Dugar - Integr. Syst. Des, 1997 - eedesign.com ... cause flip-flops to operate in metastable states and ... However, because simulation requires developing test vectors, we ... The ASIC synthesis tool we had chosen had ...

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Communication Between Independent On-Chip Synchronous Systems

I Brynjolfson - macs.ece.mcgill.ca

... N. Vijaykrishnan, "Energy Efficient Datapath **Synthesis** Using Dynamic ... and R. Brodersen, "The **Simulation** and Evaluation ... to obtain a **metastable** response from ... <u>View as HTML - Web Search</u>

A METHOD FOR HIGH RELIABILITY FIELD PROGRAMMABLE GATE ARRAY (FPGA) DESIGNS

D Albaijes, FE Branch - klabs.org

... Does timing **simulation** meet functional and performance requirements? Return to DESIGN, **SYNTHESIS**, or PLACE & ... result in **metastable** conditions at the synchronizer ... <u>View as HTML - Web Search</u>

Verifying Synchronization in Multi-Clock Domain SoC

T Kapschitz, R Ginosar, R Newton - 2004 - athdl.com

... timing violations may cause signals to go **metastable**; they also ... www.athdl.com/products. html [5] Cliff Cummings, "Simulation and Synthesis Techniques for ...

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Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs

CE Cummings - Synopsys Users Group Conference, San Jose, CA, www. sunburst ..., 2001 vlsidsp.el.yuntech.edu.tw

... detail some of the hardware design, timing analysis, synthesis and simulation methodologies to ... and might still be metastable at the next rising edge of ... Cited by 3 - View as HTML - Web Search - eecg toronto edu - all 8 versions »

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High speed externally asynchronous/internally clocked systems WS VanScheik, RF Tinder - IEEE Transactions on Computers, 1997 - ieeexplore.ieee.org ... manner similar to edge-triggered D flip-flop, but with ... Studies of the metastable condition rele- vant to this ... 7. DL-DFLOP NOR sequence recognition simulation. ... Cited by 7 - Web Search - doi.ieeecs.org - doi.ieeecomputersociety.org - portal.acm.org - all 7 versions »

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cific problem is to avoid metastable states which might drive the FSMs into unknown

... [1] Clifford E. Cummings, Peter Alfke, Simulation and Synthesis ...

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designers to add synchronizers to reduce the probability of metastable signals

... automatically finds common RTL errors, simulation-to-synthesis mismatch ...

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Development of improved constitutive models and simulation capability for processing!

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Example 6 – Verilog Asynchronous SET/RESET **simulation** and **synthesis** model ...
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